DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40240B
buffers
Octal inverting buffers with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Octal inverting buffers with 3-state outputs

HEF40240B buffers

DESCRIPTION

The HEF40240B is an octal inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs $\overline{EO}_A$ and $\overline{EO}_B$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.
Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40240B is pin and functionally compatible with the TTL '240' device.

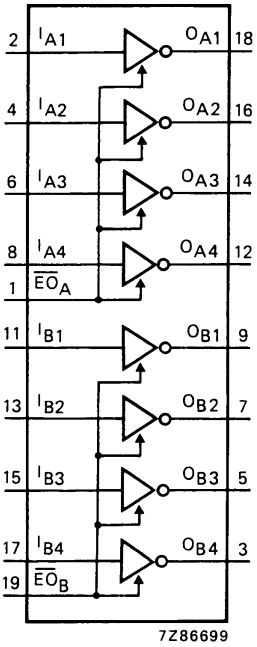


Fig.1 Functional diagram.

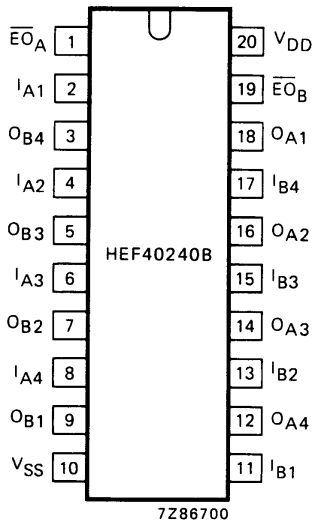


Fig.2 Pinning diagram.

HEF40240BP(N): 20-lead DIL; plastic (SOT146-1)
HEF40240BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
HEF40240BT(D): 20-lead SO; plastic (SOT163-1)
( ): Package Designator North America

PINNING

I_{A1} to I_{A4}	inputs
I_{B1} to I_{B4}	inputs
O_{A1} to O_{A4}	bus outputs
O_{B1} to O_{B4}	bus outputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs (active LOW)

FAMILY DATA, I_{DD} LIMITS category buffers

See Family Specifications

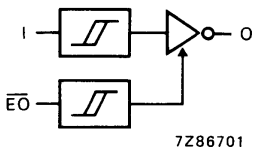


Fig.3 Logic diagram (one buffer).

TRUTH TABLE

INPUTS		OUTPUT
I_n	$\overline{EO}$	O_n
H	L	L
L	L	H
X	H	Z

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance off state

RATINGS

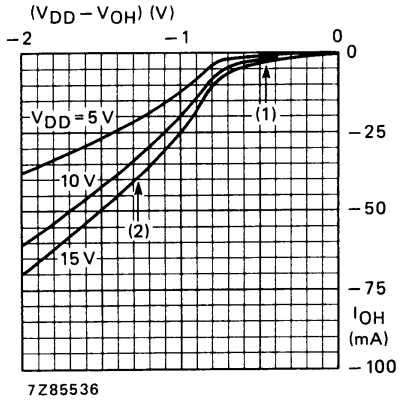
Limiting values in accordance with the Absolute Maximum System (IEC 134)
See Family Specifications except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

DC CHARACTERISTICS

V_{SS} = 0 V

PARAMETER	V_{DD}	V_{OH}	V_{OL}	SYMBOL	T_{amb} (°C)						UNIT
					−40		+25		+85		
	V	V	V		MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	
Output current	5	3,6	–	$-I_{OH}$	9,3	–	10,0	24,0	10,7	–	mA
HIGH	10	8,4	–	$-I_{OH}$	14,4	–	15,0	46,0	15,0	–	mA
	15	13,2	–	$-I_{OH}$	19,5	–	20,0	62,0	19,8	–	mA
Output current	5	4,6	–	$-I_{OH}$	0,75	–	0,6	1,2	0,45	—	mA
HIGH	10	9,5	–	$-I_{OH}$	1,85	–	1,5	3,0	1,1	–	mA
	15	13,5	–	$-I_{OH}$	14,5	–	15,0	50,0	15,5	–	mA
Output current	5	–	0,4	I_{OL}	2,9	–	2,3	5,4	1,75	–	mA
LOW	10	–	0,5	I_{OL}	9,5	–	7,6	17,0	5,50	–	mA
	15	–	1,5	I_{OL}	30,0	–	25,0	45,0	19,0	–	mA
Hysteresis	5	–	–	V_H	–	–	–	220,0	–	–	mV
voltage	10	–	–	V_H	–	–	–	250,0	–	–	mV
(any input)	15	–	–	V_H	–	–	–	320,0	–	–	mV



(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Fig.4 Typical output source current characteristic.

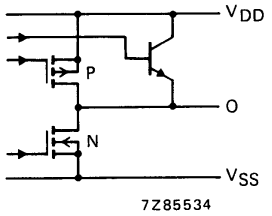


Fig.5 Schematic diagram of output stage.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

ALL BUFFERS SWITCHING	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$4\,250\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$17\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$46\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

PARAMETER	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$I_{An/Bn} \rightarrow O_{An/Bn}$	5			95	190	ns	83 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	35 ns + (0,10 ns/pF) C_L
	15			30	60	ns	26 ns + (0,07 ns/pF) C_L
$I_{An/Bn} \rightarrow O_{An/Bn}$	5			85	170	ns	82 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	38 ns + (0,03 ns/pF) C_L
	15			30	60	ns	29 ns + (0,02 ns/pF) C_L
Output transition	5			40	80	ns	see Fig.6
times	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow O_{An/Bn}$	5			70	140	ns	
HIGH	10	t_{PHZ}		35	70	ns	
	15			30	60	ns	
	5			75	150	ns	
LOW	10	t_{PLZ}		40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO} \rightarrow O_{An/Bn}$	5			80	160	ns	
HIGH	10	t_{PZH}		35	70	ns	
	15			30	60	ns	
	5			90	180	ns	
LOW	10	t_{PZL}		40	80	ns	
	15			30	60	ns	

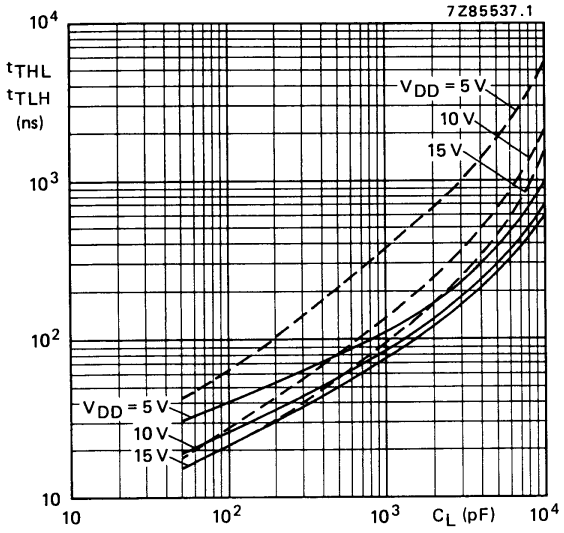


Fig.6 Output transition times as a function of the load capacitance.